A *JSSC* Classic Paper:

Low-power CMOS Digital Design

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This article is one of a series on the most frequently cited papers from the JSSC according to *The Journal Citation Report—Science Edition*. "Low-power CMOS digital design" by A. P. Chandrakasan, S. Sheng, and R. W. Brodersen originally appeared in April 1992. It is the second most frequently cited in the history of *JSSC* and is still the most recent paper of any frequently cited from *JSSC*.

Why the paper was important?

At the time of publication, the switching speed and silicon area of digital CMOS circuits were the primary design metrics used for circuit optimization. This paper brought significant awareness to design techniques that also allowed the minimization of power and energy required to perform a given computation. It identified that, in order to minimize power dissipation, the problem needed to be attacked at all levels of the design process starting from the system level, through the architectures and circuits, down to the underlying fabrication technology. Energy-optimized design has now become one of the dominant considerations in CMOS design with the ever-increasing importance of battery-operated devices and the limitations of heat removal in high-performance systems.

What was its impact?

The most significant impact of this paper was identifying the emergence of energy efficiency as a key metric in digital system design. Results from fabricated test circuits validated energy models and identified the key criteria to impact energy dissipation. The paper validated energy models with voltage scaling and presented the effect of circuit style selection, transistor sizing, and architectural optimization on energy efficiency.

The architectural voltage scaling approach (in which hardware concurrency is used to compensate for reduced throughput at lower voltages) demonstrated the ability to improve the power-delay product by an order of magnitude without performance loss and thus provided significant improvement over traditional scaling approaches. The notion of using the power supply voltage as a "free variable" met with significant skepticism when the results were first presented at workshops and at the VLSI Circuits Symposium Plenary Session. The paper solidified many of the concerns with voltage scaling and validated results with circuit demonstrations. The idea of trading-off silicon area for lower power has been used widely in academia and in industry. The techniques also have been implemented in academic and commercial CAD tools.

What inspired it and/or led up to writing it?

A large research program was underway (the Berkeley InfoPad project) to develop a portable multimedia device that supported speech recognition, video compression and decompression, pen input, and wireless communication. It quickly became evident that the required functionality could not be supported with a reasonable battery weight using traditional design approaches. Before developing the electronics for the InfoPad terminal, we decided to go back to basics and evaluate the fundamental sources of power dissipation.

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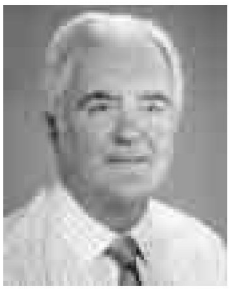
Robert Meyer Receives IEEE Graduate Teaching Award

The IEEE has named Robert Meyer as the recipient of the 2003 IEEE Leon K. Kirchmayer Graduate Teaching Award. The award recognizes Meyer for his distinguished teaching and mentoring methods, as well as the development of teaching materials for microelectronic circuit design. Meyer is the National Semiconductor Distinguished Professor at the University of California at Berkeley's department of electrical engineering and computer sciences. He is known worldwide for the distinction of his graduate students and for his text co-written with Paul R. Gray, *Analysis and Design of Analog Integrated Circuits*, in its 4th edition.



Meyer received his bachelor's degree in electrical engineering, his master's degree in engineering science, and his doctoral degree in electrical engineering from the University of Melbourne, Australia. Since joining the faculty at the University of California, Berkeley, in 1968, Meyer has supervised more than 20 doctoral students and more than 60 master's students who form a notable group of today's leading radio frequency integrated circuit designers. Additionally, many of today's leading analog bipolar IC designers have studied with Meyer.

A Fellow of the IEEE, Meyer has served the IEEE as president of the IEEE Solid-State Circuits Council and as a member of the editorial board of IEEE Press. He has earned many awards and honors, including the J.J. Thomson Premium award from the Institution of Electrical Engineers for research on noise in transistor mixers.

The award was presented on 10 February at the 2003 IEEE International Solid-State Circuits Conference in San Francisco, California. Sponsored by Olga T. Kirchmayer, the award recognizes inspirational teaching of graduate students in the IEEE fields of interest.